**1.1  What are the inputs and the outputs of RTL synthesis?**

Inputs : RTL, Technology libraries, Constraints (Environment, clocks, IO delays etc.). Outputs : Netlist , SDC, Reports etc. Design Compiler (DC) from Synopsys and RTL Compiler from Cadence are the tools widely used for synthesis. Synthesis is described as translation plus logic optimization plus mapping.

**1.2  Why do you perform Lint check during synthesis?**

**1.3  What are difference between blackbox and unresolved module on synthesis?  
1.4  Why delay model is accounted to the synthesis? What is advantage and disadvantage for the zero wire-load model?  
1.5  How to setup the synthesis tool to use more complex cell during synthesis?  
1.6  Why the high percentage of sequence cells effect to your design?  
1.7  What do you need to perform physical-aware synthesis?  
1.8  What is advantage of early clock planning on synthesis?  
1.9  How to check and optimize of clock gater during synthesis?  
1.10What is scan-def? why do you need scan-def?  
1.11 How can you validate the scan-def?**

**2.1  What are based timing constraint for DRV checks?  
2.2  What are based constraint for a synchronous design?  
2.3  What are asynchronous timing paths? What are based constraints for those paths?  
2.4  What are based constraint to be applied to a memory?  
2.5  How to debug timing critical path?  
2.6 How to create a phrase-shift timing constraint for a clock?  
2.7 Can you draw some diagram and explain how to create a generated clock of divider by 3 for 1Ghz clock?  
2.8 What type of checks that can be done in STA timing analysis tool?  
2.9  How to develop the correct timing exception constraint?  
2.10 How can you calculate the FIFO depth?  
2.11 How do you resolve the timing issue of a combinational loop?  
2.12 What are difference between min pulse-width and min period check? Why do you need those checks?  
2.13 What is clock uncertainty? How much clock uncertainty do you have in your design?  
2.14 What is temperature inversion?  
2.15 What is a look-up table? can you explain a 2D table?  
2.16 What is synchronizer flop? Is there any timing check with synchronizer flop?  
2.17 What are virtual clocks? Why are they used?**

**3.1  What are the inputs and outputs of Floorplanning?  
3.2  How will you decide the best floorplan?  
3.3  What is keep-out margin?  
3.4  How to do the design partitioning?  
3.5  What are advantages and disadvantages of flat design?  
3.6  What is the concept of design rows in the floorplan?  
3.7. How many layers do you have in your design?  
3.8. Why the power stripes always route on top metal layer?  
3.9. What are difference between base layers and metal layers?  
3.10 What are difference between preferred routing track and preferred routing track?  
3.11 How to do integrate a hardening IP like Serdes, DDR PHY into your design?  
3.12 What is multi-driven net?  
3.13 How to do the timing budgeting?  
3.14 How to do pin alignment on a hierarchical design?  
3.15 What are differences between Bump and Bond-pad?  
3.16 How to decide a good bump pitch?**

**4.1  What are the inputs and type output of power planning?  
4.2. How to design a power grid?  
4.3 What is power rail?  
4.4  What is power mesh (stripe)?  
4.5  What is a flip-chip design?  
4.6. Why I/O cells are place in the design?  
4.7  What are main difference between a FinFET and Planar-FET technology?  
4.8  What is metal slotting?  
4.9  What is a power switch cell?  
4.10 What is a level-shifter cell?  
4.11 What is the use of isolation cell?  
4.12 What is electromigration (EM)? And how to fix it?  
4.13 What is IR drop analysis? Why do you need it?  
4.14 What are difference between static IR drop analysis, Vector-less and VCD based analysis?  
4.15 What are the inputs of VCD based power analysis?**

**5.1. What are major differences between 16nm technology node and 28nm technology node?  
5.2. What are major differences between 7nm technology node and 16nm/14nm technology node?  
5.3. What are major differences between 5nm technology node and 7nm technology node?  
5.4. What are the new design rules in 7nm technology node?  
5.5. What is cut metal layer?  
5.6. What is double patterning?  
5.7. What is via pillar?  
5.8. What does CNOD stand for?  
5.9. What are difference between full-colored DPT and colorless DPT?**

**6.1  What are inputs and output of placement?  
6.2. What are types of placement grid?  
6.3. What are the types of placement blockages? Can you explain the use of a partial placement blockage?  
6.4. What are types of routing blockages?  
6.5. What is the use of ESD cell?  
6.6. What are difference between WELL-TAP cells and ENDCAP cells?  
6.7. What is a latch-up violation? How to prevent latch up?  
6.8. What is the checker-board placement for well-tap? is it one of optimum methodology?  
6.9. What is scan chain reordering? Why do you need perform scan chain reordering at placement step?  
6.10 What is the magnetic placement? Give an example of when and where do you need it?  
6.11 What do you need to pre-route a bus?  
6.12 What is advantage and disadvantage of Manhattan based timing analysis during placement?  
6.13 Why do you need fix the local cell placement density issue?  
6.14 What do PPA stands for?  
6.15 What does power-recovery do for your design?  
6.16 What is routing congestion? How to fix it?  
6.17 How do you place memory, hard macro in your design?  
6.18 Why do you need early useful skew in placement step?  
6.19 How do you decide a best placement?  
6.20 What are the type logic optimizations? Give some method of logic optimization?  
6.21 Why do high-layer routing promotion help improve timing?  
6.22 What is spare cell? When do you use it?  
6.23 What is Early Clock Flow (ECF)? What are the benefits of ECF?  
6.24 What is back-2-back diode? When and where do you use it?**

**7.1  What are the inputs and the outputs of Clock-tree synthesis (CTS)?  
7.2  What are difference between setup violation and hold violations?  
7.3. Why hold fixing is the more importance than setup?  
7.4. What is the cross-talk?  
7.5. Why inverters are used in the clock tree?  
7.6. What is non-default rule (NDR)? why do you need NDR?  
7.7. What is clock shielding?  
7.8. How cell delay vary with different PVT conditions?  
7.9. What are xtalk aggressor and victim?  
7.10 How to fix SI glitch?  
7.11 What is clock transition violation?  
7.12 What is clock latency? How to reduce the clock latency?  
7.13 How to design a zero skew clock tree?  
7.14 What are advantage and disadvantage of smaller skew clock-tree synthesis?  
7.15 What are difference between multi tap H-tree and clock mesh?  
7.16 What are the type of clock topology?  
7.17 How shielding help avoid crosstalk problem? What exactly happens there?  
7.18 What is on-chip variation?  
7.19 What is a multi-mode, multi-corner design?  
7.20 What are differences between fixed derate OCV and P-OCV?  
7.21 How CRPR account to the timing analysis?  
7.22 What are useful skew? Why do you need useful skew?**

**8.1  What are the inputs and the output of Routing?  
8.2  What are the types of physical verification?  
8.3  What is dishing effect?  
8.4  What is etching?  
8.5  What is wire spreading?  
8.6  What are the violations solved in LVS?  
8.7  What does we do for low power design?  
8.8  What is CMP (chemical mechanical polishing)?  
8.9  Did you get antenna violation in your design? How to fix it?  
8.10 Why metal density rule are important?  
8.11 What is metal fill insertion?  
8.12 What is analysis do you need with metal-filled design?  
8.13 What are types of ERC violations?  
8.14 How do you reduce the power consumption by using low-Vth and high-Vth?  
8.15 What is chip yield? Why design density and floorplan shape matter to chip yield?  
8.16 How to fix a signal EM violation?  
8.17 How to prevent latch-up violation?  
8.18 How do importance of short violation and metal spacing violation?  
8.19 What are multi-bits flop? What are advantages of multi-bits flops?  
8.20 What is via-pillar and how via pillar help improve PPA of your design?  
8.21 What is floating poly gate check?  
8.22 What is GDS merging? Why do you need it?  
8.23 What is kind of base-fill insertion?  
8.24 Why do you need redundant via insertion?**

**9.1. What are the inputs and outputs of RC extraction?  
9.2. What is delay back-annotation? How to do it?  
9.3  What are the inputs and the outputs of Logic Equivalence Check (LEC)?  
9.4. What are types of LEC issue you have seen in your design? and how to fix it?  
9.5. What are types of LEC un-mapping points?  
9.6. Common areas where LEC fails?  
9.7. How does .lib file (Liberty format) take account to the LEC check?  
9.8. What are difference between Non-equivalence and inverted-equivalence?  
9.9  How to use spare-cell to do a metal layer ECO?  
9.10What are differences between the STA and DTA?  
9.11 If we increase the fan-out of the cell how it will effects delay?  
9.12 If you have both congestion and Irdrop violation, how do you fix them?  
9.13 In reg2reg setup violation, where do you insert buffer to fix them, near lauching flop or near capturing flop? And why?  
9.14 What can you do to fix hold violation if we are freezing base layer?  
9.15 Can you talk about low power techniques? How low power and deep submicron techniques are related?  
9.16 What are difference between graph based timing analysis and path based timing analysis?  
9.17 How to fix a slew limit violation?  
9.18 How to fix setup and hold violation?  
9.19 If you have a timing short path that violate both setup and hold, how to you solve it?  
9.20 What does max-length constraint account for PnR tool?  
9.21 What is the max-delay constraint? How to fix the max delay timing violation?**

**9.22 What does LEF file contain?**

**9.23 What does LIB file contain?**

**9.24 What are differences between SPEF and SDF?**

**9.25 Why do you need SDF file?  
9.26 What are the setup and hold edges for the half-cycle path?  
9.27 What are the setup and hold edges for the positive latch to negative flop?  
9.28 How to apply the OCV derate to your design?  
9.29 Why do you need difference derate for capturing and launching paths?  
9.30 What is a lock-up latch? How does it help on timing fixing?  
9.31 What is timing credit slice? How timing credit slice help on timing closure?**